A HIGH EFFICIENCY FREQUENCY DOUBLER FOR 100 GHz

Marek T. Faber† and John W. Archer††

National Radio Astronomy Observatory*
2015 Ivy Road
Charlottesville, Virginia 22903

Robert J. Mattauch

University of Virginia
Charlottesville, Virginia 22901

ABSTRACT

Development of a high efficiency varactor frequency doubler for 100 GHz is reported. The efficiency of the doubler is greater than 32% at any frequency between 97 GHz and 102 GHz and reaches 35% at 98 GHz. This is the highest efficiency ever reported for a frequency multiplier above 75 GHz. The measured efficiency is in very good agreement with a theoretically predicted value. The doubler is very suitable for the realization of a W-band, all solid-state, local oscillator source.

INTRODUCTION

In recent years, frequency multipliers have become widely used to provide a reliable, low-cost source of local oscillator power in millimeter wavelength heterodyne receivers. In many applications, particularly if a solid-state generator is to be used as a driving source, the power available at the input frequency is limited to several milliwatts and an efficiency of frequency conversion is of primary importance. Development of a high efficiency varactor frequency doubler for 100 GHz is reported in this paper.

THEORETICAL PREDICTIONS

Both diode and mount design play important roles in maximizing the efficiency of a varactor frequency multiplier. The efficiency is determined by an efficiency of frequency conversion, η_d, and losses α_{in} and α_{out} in input and output circuits of the multiplier mount:

$$\eta = \alpha_{in}\,\eta_d\,\alpha_{out} \quad .$$

An accurate determination of the efficiency of frequency conversion, η_d, is only possible if the mount embedding impedances are known at all pump harmonics. It is usually necessary to construct a low frequency scale model in order to measure them. However, an analysis of a simplified model of a varactor doubler mount can be useful, as it can illustrate what must be done to maximize efficiency. Analysis of the idealized doubler allows the derivation of the limit η_{dmax} imposed on conversion efficiency. The analysis was carried out with the following simplifying assumptions:

1) The pump circuit is conjugately matched to the diode impedance at the pump frequency (50 GHz).

2) The output waveguide is perfectly decoupled from the pump circuit by the low-pass filter and the filter presents a short circuit to second and higher order pump harmonics at the guide wall.

3) The diode is represented by the series connection of a resistor R_s = 10 Ω and a nonlinear capacitance which obeys the law

$$C(V) = C_o(1 - V/\phi)^{-\frac{1}{2}}$$

where C_o = 20 fF is the zero bias capacitance, V is the applied voltage, and ϕ = 0.92 V.

4) The output waveguide tuning short is adjusted for maximum second harmonic conversion efficiency. This is achieved when the varactor reactance is resonated out by the mount at the output frequency (100 GHz).

The mount impedances seen by the diode at the first five pump harmonics were determined using the techniques described in (1). The current and voltage waveforms were then derived by a nonlinear analysis technique, a modified version of the computer method described in (2). The pump drive was small enough (P_{in} = 10 mW) to avoid forward current flow in the varactor and not to exceed the reverse breakdown

† On leave from the Institute of Electronics Fundamentals, Warsaw Technical University, Nowowiejska 15/19, 00-665 Warsaw, Poland.

†† Currently with CSIRO, Division of Radiophysics, P. O. Box 76, Epping, NSW, Australia 2121.

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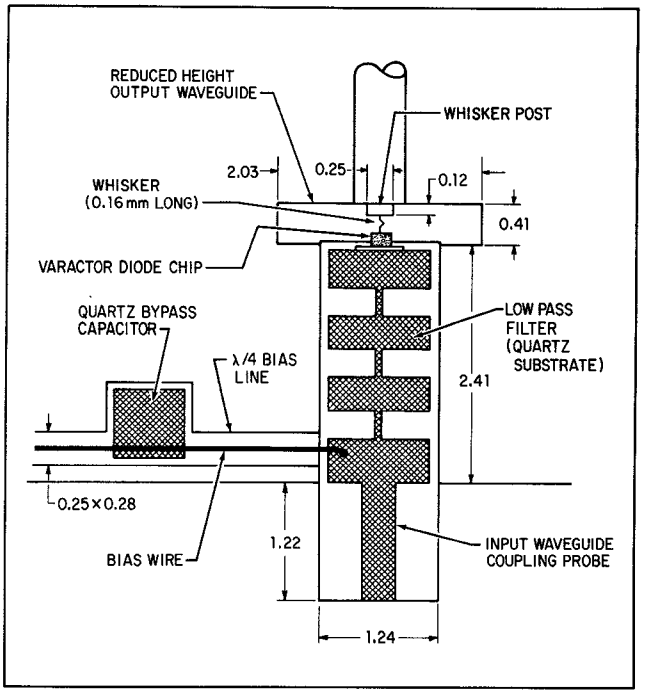
voltage. The efficiency calculations showed that η_{dmax} = 49% is possible for the idealized doubler analyzed when output waveguide height is reduced by the factor of 0.4.

DOUBLER MOUNT

A practical doubler mount was developed from a design described previously (3). The split-block, crossed-waveguide mount is shown schematically in Figure 1. Pump power, incident in the full height WR-15 input waveguide, is fed, via a waveguide-to-stripline transition (4), to a suspended substrate stripline low-pass filter, fabricated on crystalline quartz 0.076 mm thick. The seven-section filter passes the fundamental frequency with low loss, but is cut off for higher order harmonics. The low-pass filter also transforms the impedance of the pumped varactor at the input frequency to a convenient value at the plane of the waveguide-to-stripline transition. Pump circuit impedance matching is achieved using a sliding contacting backshort.

The varactor diode chip is mounted in the reduced-height WR-8 output waveguide which provides Z_o = 226 Ω at 100 GHz. The diode is contacted by a 12.7 μm diameter, gold-plated, phosphor-bronze whisker attached to a gold-plated, BeCu alloy pin which is an interference fit in the doubler



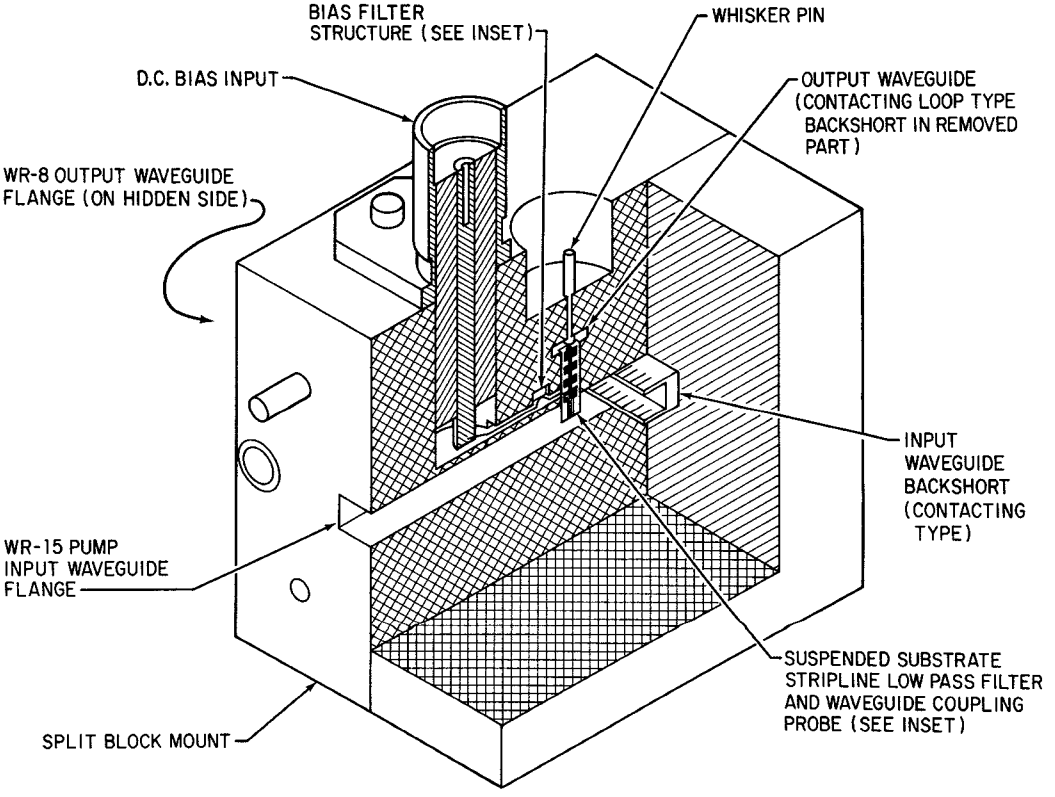


Fig. 1. An isometric drawing and sketch showing the main features of the doubler design and details of the varactor mounting and biasing structure. Dimensions are in mm.

body. The mount is matched to the impedance of the diode at the second harmonic of the pump with the aid of an adjustable contacting loop type backshort (5) in the reduced height guide. A quarter-wave, three-section, step impedance transformer is used to couple the reduced-height guide to the full-height output waveguide.

DC bias is brought to the diode via a transmission line bias filter. The outer shield of the bias line is a rectangular cross section channel milled into the surface of one of the blocks forming the mount. The center conductor is a length of 25 μm diameter gold wire bonded at one end to a low impedance section of the low-pass filter. The line is then connected to a 100 fF metallized quartz dielectric bypass capacitor. The line terminates on the center pin of the SMA bias connector.

The varactor diode used in the doubler is a GaAs Schottky barrier diode fabricated at the University of Virginia. The diode, a designated type 6P2, has typical zero bias capacitance of 20 fF, a DC series resistance of 10 Ω, a breakdown voltage of 18 V, a saturation current of $2 \cdot 10^{-17}$ A, an ideality factor of 1.1 and ΔV = 0.065 V.

The mount is estimated to have the following losses: 0.1 dB in the input waveguide; 0.1 dB in the input sliding backshort; 0.3 dB in the waveguide-to-stripline transition and the low-pass filter; 0.15 dB in the reduced height output waveguide and the sliding backshort; and 0.25 dB in the output waveguide transformer. This gives total losses of 0.5 dB (α_{in} = 0.891) and 0.4 dB (α_{out} = 0.912) in the mount input and output circuits, respectively. Thus, the efficiency of the doubler might be expected to be as high as

$$\eta_{max} = \alpha_{in}\, \eta_{dmax}\, \alpha_{out} = 39.8\%$$

if the practical doubler approached the idealized case analyzed.

DOUBLER PERFORMANCE

The performance of the initially assembled doubler was measured and compared with the predicted limit. Then fine changes to the diode embedding circuit were made and the doubler performance reevaluated (Figure 2). The whisker post diameter was finally reduced to 0.25 mm, the length of the post in the guide increased to 0.12 mm and the whisker length shortened to 0.16 mm (see Insert of Figure 1). These have resulted in the doubler performance shown in Figure 2 curve 3 and Figure 3. Bias and tuning were adjusted for best performance at each measurement frequency and each pump level. For a 5 mW input power the efficiency of the doubler is greater than 32% at any frequency between 97 and 102 GHz and reaches 35% at the frequency of 98 GHz. This is the highest efficiency ever reported for a frequency multiplier above 75 GHz. (η = 25% at 100 GHz was reported in (6) and η = 27% at 215 GHz in (7).)

The relationship between pump power and efficiency is illustrated graphically in Figure 3 for the frequency of 98 GHz. The conversion efficiency of the doubler reaches its maximum value of 35% at 5 mW input power and then begins to decrease as the pump power level is increased. This is because of the loss associated with forward current flow in the varactor.

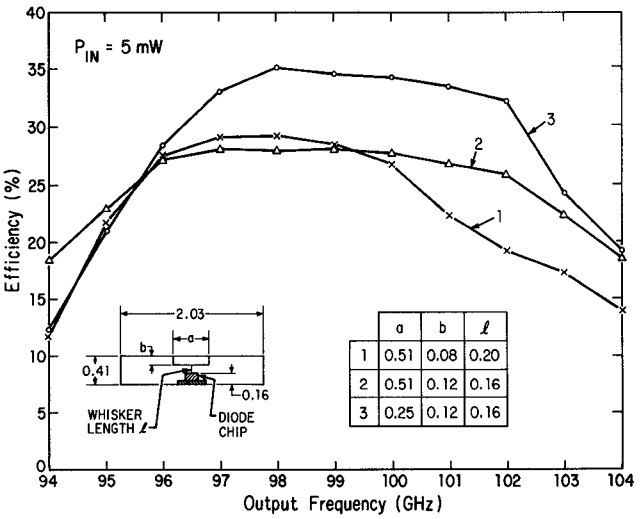


Fig. 2. Conversion efficiency of the doubler versus output frequency for three different varactor mounting structures. DC bias and tuning were optimized at each measurement frequency.

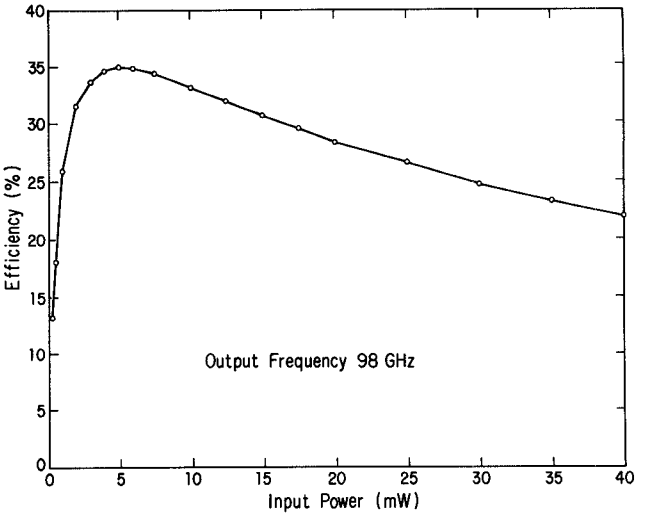


Fig. 3. Conversion efficiency of the doubler versus pump power for the final diode mounting structure (case 3 in Fig. 2). DC bias and tuning were optimized at each pump power.

For the first time very good agreement between measured and theoretically predicted performance of a millimeter-wave frequency multiplier has been achieved. The small discrepancy between measured η = 35% and predicted η = 39.8% is due to the fact that the practical doubler does not fully satisfy the simplifying assumptions made in the analysis. In particular, the zero bias junction capacitance of the diode was measured to be 26 fF instead of the assumed 20 fF and capacitance versus voltage response, shown in Figure 4, was less nonlinear than the response of an ideal abrupt junction assumed in the analysis. If these had been accounted for in the analysis, the predicted conversion efficiency η_{dmax} would have been lower in the given mount.

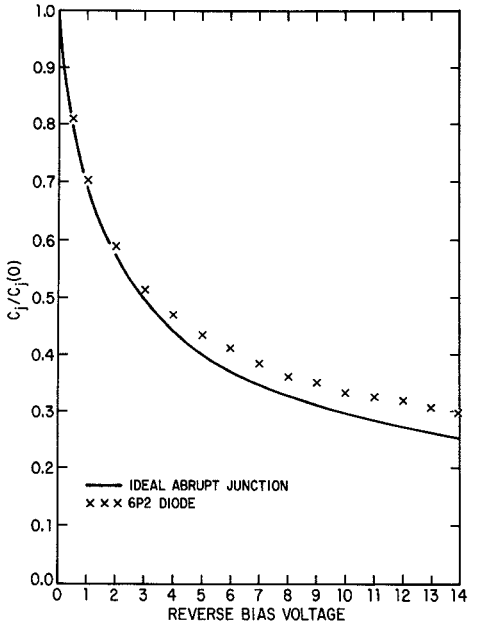


Fig. 4. Normalized junction capacitance versus reverse voltage for an ideal abrupt junction varactor used in the analysis and for the 6P2 diode (measured).

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